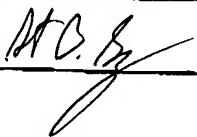


Sheet 1 of 3

<b>FORM PTO-1449 (SUBSTITUTE)</b>  U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE  <b>INFORMATION DISCLOSURE          STATEMENT BY APPLICANT</b> (37 CFR 1.98(b))				Attorney Docket No.: P2001,0216 Appl. No.:  Applicant: ANNALISA CAPPELLANI ET AL.  Filing Date: September 26, 2003 Group Art Unit: <b>2829</b>			
EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
SBG	A	6,091,120	7/18/00	Yeom et al.	—	—	
SBG	B	5,089,863	2/18/92	Sato et al.	—	—	
SBG	C	5,384,479	1/24/95	Taniguchi	—	—	
	D						
	E						
	F						
	G						
	H						
	I						
<b>FOREIGN PATENT DOCUMENT</b>							
		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES   NO
SBG	J	42 34 528 C2	4/15/93	Germany	—	—	X
	K	42 34 777 A1	4/21/94	Germany	—	—	X
	L	2 791 177 A1	9/22/00	France	—	—	
	M	63044768	2/25/88	Japan	—	—	X
SBG	N	0 740 334 A2	10/30/96	Europe	—	—	X
<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)</b>							
SBG		Widmann, D. et al.: "Technologie hochintegrierter Schaltungen" [Technology of High-Density Integrated Circuits], Springer Verlag, 2 <sup>nd</sup> Edition, pp. 201-203					
SBG		Ghani, T. et al.: "100nm Gate Length High Performance/Low Power CMOS Transistor Structure", IEEE, 1999, pp. 415-418					
EXAMINER				DATE CONSIDERED			
				6.7.04, 7/28/04			

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<b>FORM PTO-1449 (SUBSTITUTE)</b>				Attorney Docket No.: P2001,0216			
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE				Appl. No.:			
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				Filing Date: September 26, 2003			
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EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
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FOREIGN PATENT DOCUMENT							
		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES   NO
586	J	0 328 350 A2	8/18/89	Europe	—	—	X
586	K	02/41383 A1	5/23/02	WIPO	—	—	X
	L						
	M						
	N						
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)							
586		Lasky, J. B. et al.: "Comparison of Transformation to Low-Resistivity Phase and Agglomeration of $\text{TiSi}_2$ and $\text{CoSi}_2$ ", IEEE Transactions on Electron Devices, Vol. 38, No. 2, February 1991, pp. 262-269					
586		Hisamoto, D. et al.: "A Low-Resistance Self-Aligned T-Shaped Gate for High-Performance Sub-0.1- $\mu\text{m}$ CMOS", IEEE Transactions on Electron Devices, Vol. 44, No. 6, June 1997, pp. 951-956					
EXAMINER				DATE CONSIDERED			
100.12				6.7.04, 7/28/04			

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<b>FORM PTO-1449 (SUBSTITUTE)</b>		<b>Attorney Docket No.: P2001,0216</b>					
<b>U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE</b>		<b>Appl. No.:</b>					
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))</b>		<b>Applicant: ANNALISA CAPPELLANI ET AL.</b>					
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<b>EXAMINER INITIALS</b>		<b>PATENT NO.</b>	<b>DATE</b>	<b>PATENTEE</b>	<b>CLASS</b>	<b>SUB CLASS</b>	<b>FILING DATE</b>
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		<b>DOCUMENT NO.</b>	<b>DATE</b>	<b>COUNTRY</b>	<b>CLASS</b>	<b>SUB CLASS</b>	<b>TRANSL. YES / NO</b>
	J						
	K						
	L						
	M						
	N						
<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)</b>							
<i>SB6</i>		Kasai, K. et al.: "W/WNx/Poly-Si Gate Technology for Future High Speed Deep Submicron CMOS LSIs", IEEE, 1994, pp. 497-500					
<b>EXAMINER</b>	<i>H.C. Bz</i>			<b>DATE CONSIDERED</b>			
				<i>6.7.04, 7/20/04</i>			

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